

PC Engines

WRAP router platform

Version WRAP.1A

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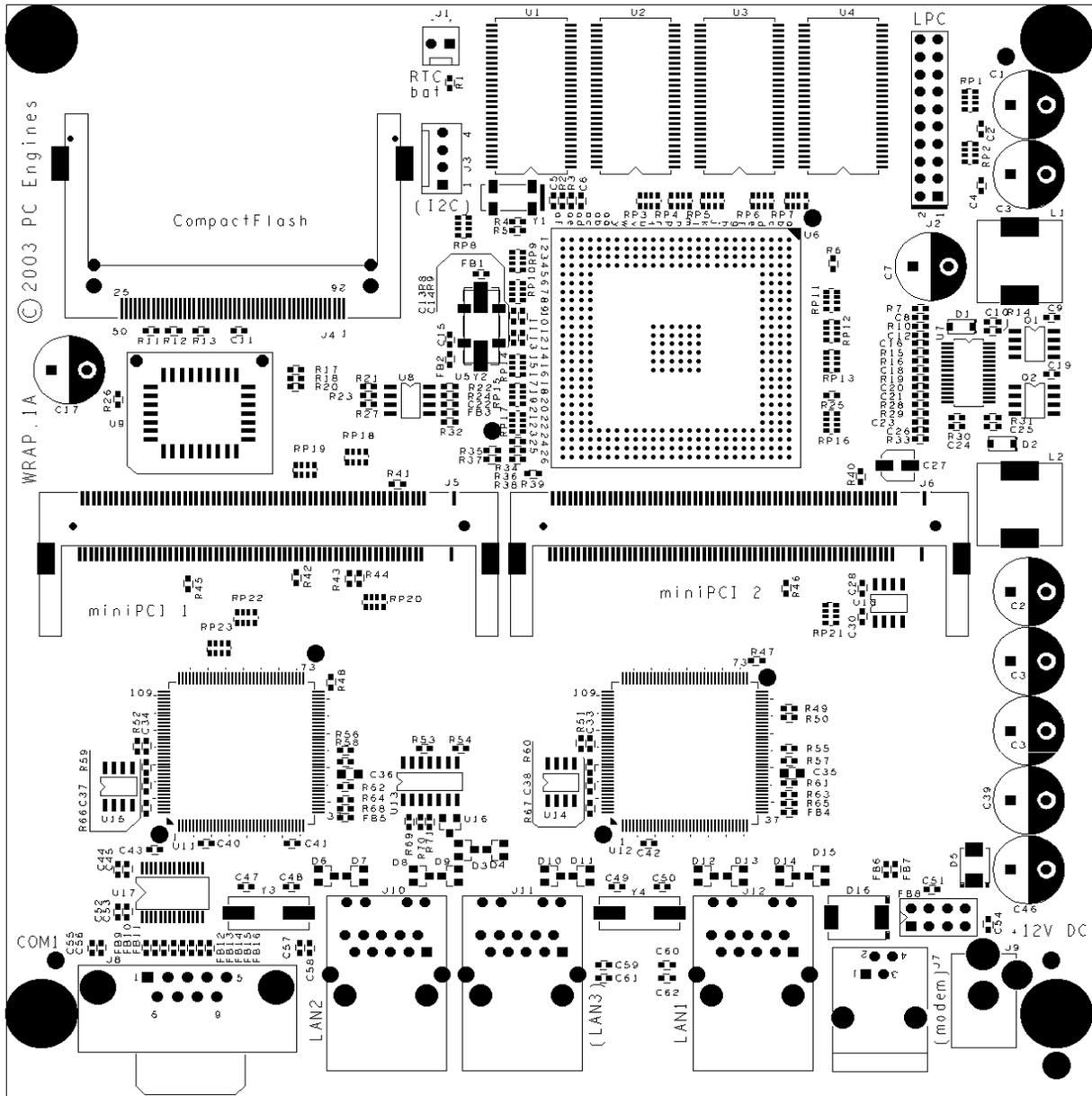
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# Introduction

Thank you for testing the PC Engines WRAP platform for your networking application.

WRAP is a small single board computer optimized for wireless access and network routing applications.



## Features

- National SC1100 CPU, 266 MHz 5x86 CPU, 16KB cache
- 2 Ethernet channels (National DP83816)
- 2 miniPCI sockets for 802.11 wireless cards and other expansion (better performance than CardBus, should be lower cost soon)
- 64 MB SDRAM, 64 bit wide for higher memory bandwidth compared to AMD ElanSC520 based boards.
- 128 KB flash for tinyBIOS system BIOS, enough space left for network boot
- CompactFlash header for user's operating system and application
- 12V DC supply through DC jack or passive power over LAN 1 connector
- 1 serial port (DB9 male)
- Watchdog timer built into SC1100 CPU
- LM77 thermal monitor
- Header for optional RTC battery (future versions)
- Header for I2C bus (can be used for front panel interface)
- Header for LPC bus (can be used for I/O expansion)

## OEM options

The following options can be configured for larger orders:

- DRAM size (32 MB, 64 MB, 128 MB)
- CPU speed (233 MHz, 266 MHz, future 300 MHz)
- 1 or 2 Ethernet channels
- 1 or 0 Serial ports
- Support for third Ethernet channel using a custom miniPCI card and on-board RJ45.
- Support for miniPCI modem (must have own data pump, not a AC97 modem), on-board RJ11.
- 3 front panel LEDs + 1 switch (next version)
- BIOS adaptations as needed
- Passive power feed adapter POE.1A

## Technical data

Power supply	+12V DC, ~ 0.25A halt, ~0.5A active (excluding miniPCI cards)
Temperature range	0 to 50°C (this range may be extended by using a CPU heat sink, and changing to 233 MHz)
Dimensions	6 x 6" (152.4 x 152.4 mm)

## Getting started...

- Connect a +12V power supply to the DC jack J9. A suitable power supply would be e.g. CUI Stack DPS120125P5P (Digi-Key part T923-P5P-ND).
- Connect the serial console using a null modem or Laplink cable. Serial port parameters are 9600 8N1.
- Insert CompactFlash card with your operating system and application in CompactFlash header J4.
- Power on...

You should see tinyBIOS startup messages, memory size, CF disk geometry on the serial console.

## CompactFlash partitioning

The current version of tinyBIOS is set up to configure the CF card in LBA mode. If there are problems, please compare the LBA parameters shown on startup with those shown on your development system where the CF card was configured.

I am considering to add autodetection of CHS / LBA mode based on the geometry in the partition sector.

If you need CHS mode now, please contact me for an alternate BIOS.

## Thermal sensor

The thermal sensor will reset the system when the temperature exceeds a critical level (power on default = 80C). Reset will be released when the temperature goes back down.

The LM77 thermal sensor sits on the secondary I2C bus, at address 90h. DOS based sample code is available on request. National also has a Linux driver for the I2C, but I'm not so sure it is any good.

## Support

This is a new product – please expect some bumps in operating system installation.

Please feel free to contact me at reasonable hours (7am to 11pm middle European time = GMT + 1 or +2) at +41 43 268 9817, or at [pdornier@pcengines.ch](mailto:pdornier@pcengines.ch) !

## FreeBSD

The default FreeBSD boot sector expects a keyboard controller to be present. This will hang on the WRAP board.

Modify `src/sys/boot/i386/boot2/boot1.s` to skip this routine (e.g. patch in a `ret` instruction).

```
//  
// Enable A20 so we can access memory above 1 meg.  
//  
seta20:   cli                               // Disable interrupts  
seta20.1: inb $0x64,%al                      // Get status  
          testb $0x2,%al                    // Busy?  
          jnz seta20.1                      // Yes  
          movb $0xd1,%al                    // Command: Write  
          outb %al,$0x64                    //  output port  
seta20.2: inb $0x64,%al                      // Get status  
          testb $0x2,%al                    // Busy?  
          jnz seta20.2                      // Yes  
          movb $0xdf,%al                    // Enable  
          outb %al,$0x60                    //  A20  
          sti                               // Enable interrupts  
          retw                              // To caller
```

Other changes are probably needed...

# Linux

Boots ok. Kernel should be configured not to look for a keyboard controller to avoid error messages.

# RxDOS

RxDOS is a free DOS-compatible operating system written by Michael Podanoffsky. Used for functional testing and firmware upgrade.

Full A386 source code and binary can be found at <http://os.drake3d.com/> .

Recommended procedure to install on a CompactFlash card:

1. Select translation mode for the CF card to be LBA.
2. Clear partition sector using a disk editor if necessary.
3. Create partition with FDISK. If the CompactFlash card is drive C, make partition active.
4. Reboot, then FORMAT partition.
5. If the CompactFlash is drive D, use the partition editor EDPART (download from Simtel) to make the partition active.
6. Modify mk\_boot.bat (RxDOS bin directory) as needed, execute it:

```
makerxd_boot -1 -s d
copy ..\rxdosbio\rxdosbio.sys d:
copy ..\rxdos\rxdos.sys d:
copy ..\rxdoscmd\rxdoscmd.com d:
copy autobat d:\autoexec.bat
```

# Connector pinouts

## J1 RTC battery

An external RTC battery can be connected here. Please note that National recommends to ground the battery input on the A3 revision of the SC1100 CPU, so a shunt is installed normally. Battery drain of the SC1100 CPU is relatively high, so a reasonably large battery should be used.

1	VBAT	battery + (3V Lithium battery)
2	GND	battery -

## J2 LPC expansion

The LPC port can be used to connect a super I/O device, or for an alternate flash EPROM to start with a corrupted or blank flash EPROM on board.

1	PCLK2	LPC clock (33 MHz)
2	GND	ground
3	LAD0	LPC data 0
4	GND	ground
5	LAD1	LPC data 1
6	GND	ground
7	LAD2	LPC data 2
8	GND	ground
9	LAD3	LPC data 3
10	GND	ground
11	LFRAME#	LPC frame
12	GND	ground
13	PCIRST#	reset (active low)
14	NC	reserved
15	LPCISP	high to use LPC flash, low to use on-board flash, pulled low by resistor
16	NC	reserved
17	GND	ground
18	V3	+3.3V supply
19	SERIRQ	serial interrupt
20	LDRQ#	LPC DMA request

## J3 I2C header

This header can be used to connect user specific hardware, e.g. a front panel microcontroller.

1	+3.3V	power supply
2	SCL1	I2C clock
3	SDA1	I2C data
4	GND	ground

## J4 CompactFlash

The CompactFlash card is used in True IDE mode. Hot insertion is not supported – please power off the unit before inserting a CF card.

1	GND	ground
2	D3	IDE data
3	D4	IDE data
4	D5	IDE data
5	D6	IDE data

6	D7	IDE data
7	CS0#	IDE decode (1F0..1F7)
8	A10	ground
9	ATASEL#	ground to select true IDE mode
10	A9	ground
11	A8	ground
12	A7	ground
13	VCC	+3.3V power supply
14	A6	ground
15	A5	ground
16	A4	ground
17	A3	ground
18	A2	IDE address
19	A1	IDE address
20	A0	IDE address
21	D0	IDE data
22	D1	IDE data
23	D2	IDE data
24	IO16#	16 bit decode, not connected
25	CD2#	card detect, not connected
26	CD1#	card detect. not connected
27	D11	IDE data
28	D12	IDE data
29	D13	IDE data
30	D14	IDE data
31	D15	IDE data
32	CS1#	IDE decode (3F6..3F7)
33	VS1#	not connected
34	IOR#	IDE read strobe
35	IOW#	IDE write strobe
36	WE#	connected to +3.3V
37	IRQ	IDE interrupt
38	VCC	+3.3V power supply
39	CSEL#	cable select, ground = master
40	VS2#	not connected
41	RESET#	IDE reset, active low
42	IORDY	IDE ready
43	INPACK#	not connected
44	REG#	connected to +3.3V
45	DASP#	pulled up
46	PDIAG#	pulled up
47	D8	IDE data
48	D9	IDE data
49	D10	IDE data
50	GND	ground

The CompactFlash specification can be found at [www.compactflash.org](http://www.compactflash.org).

### **J5, J6 miniPCI sockets**

These sockets implement the miniPCI interface. Please see schematic excerpts for pinout.

J5 can connect to the third LAN port (J11), and to AC97 audio codec signals. To implement the third LAN port, ESD diodes (BAV99) and the RJ45 / magnetics module need to be installed. This is intended for use with a custom miniPCI card.

J6 can connect to the modem port J7. To use this, the RJ11 connector would need to be populated. Because of CPU speed constraints, a modem card with internal data pump should be used. AC97 based modems are not suitable.

Please note that the current available from the +5V supply is very limited, and generated very inefficiently (linear regulator from input supply). This should be used as a bias voltage only.

### **J7 Modem connector**

This RJ11 connector can be installed to support a miniPCI modem card.

1	NC	not connected
2	TIP	phone line tip
3	RING	phone line ring
4	NC	not connected

### **J8 Console serial port**

The standard PC pinout is used. To connect to a PC, use a null modem or "Laplink" cable.

1	DCD	data carrier detect (input)
2	RXD#	receive data (input)
3	TXD#	transmit data (output)
4	DTR	data terminal ready (output)
5	GND	ground
6	DSR	data set ready (input)
7	RTS	ready to send (output)
8	CTS	clear to send (input)
9	RI	ring indicator (input)

### **J8 DC power jack**

This is a generic DC jack connector with a 2.1mm center pin. For the current revision, valid input voltage range is +7 to +13.2V. Supply current is about 0.45A at 12V, without any miniPCI adapters.

center	VIN	+12V input voltage
sleeve	GND	ground

### **J12 Ethernet port 1**

A RJ45 connector with integrated magnetics is used. This port implements a passive power over Ethernet scheme over the two unused pairs.

1	TX+	transmit positive
2	TX-	transmit negative
3	RX+	receive positive
4	VCC	power supply (nominal 12V)
5	VCC	"
6	RX-	receive negative
7	GND	power return
8	GND	"

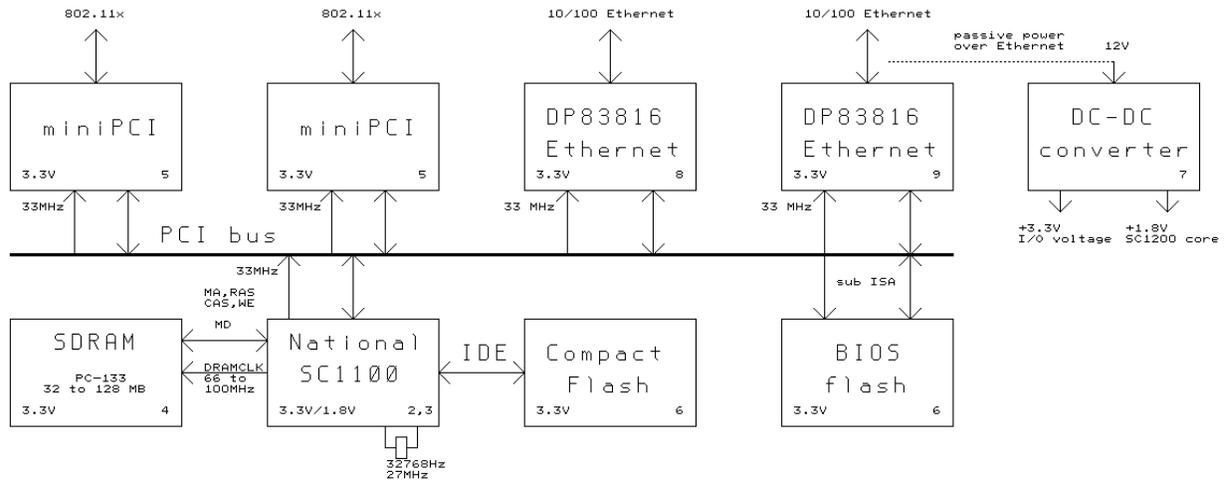
### **J10, J11 Ethernet ports 2, 3**

A RJ45 connector with integrated magnetics is used. J11 is optional, for the third Ethernet port. These ports do NOT support power over Ethernet.

- 1 TX+ transmit positive
- 2 TX- transmit negative
- 3 RX+ receive positive
- 4 NC not connected
- 5 NC not connected
- 6 RX- receive negative
- 7 NC not connected
- 8 NC not connected

## Block diagram

Full schematics can be made available to qualified customers under NDA.





## POST codes

tinyBIOS writes POST / diagnostic codes to port 80h. To make these codes visible, use a miniPCI POST card such as PC Engines POST.5A. POST codes are:

01	reset entry
02	chipset initialization
03	detect base memory size
04	initialize shadow RAM
05	init mono video
06	disable PCI devices
07	test low 64KB of DRAM
08	initialize stack
09	BIOS checksum
0a	super I/O initialization
0b	RTC test
0c	refresh / 8254 test
0d	speed-dependent chipset regs
0e	test 8237 DMA
0f	test DMA page registers
10	test 8254 registers
11	test keyboard controller
12	init timer, DMA, 8259...
13	test 8259 mask registers
14	test low 640KB
15	init vectors
16	PCI plug & play
17	shadow video BIOS
18	look for VGA BIOS
19	sign-on prompt
1a	second keyboard test
1b	extended memory test
1c	enable interrupts
1d	test / init RTC
1e	init floppy disk
1f	option ROM scan
20	test parallel ports
21	test serial ports
22	enable coprocessor
23	floppy init
24	hard disk init
25	PS/2 mouse detect
26	timer/RTC check
27	OEM boot decision point
00	boot
33	NMI
F7	low 64KB memory test failed

# Resources

## Tools

POST cards, CompactFlash adapters, CompactFlash cards and other accessories are accessible from PC Engines. Visit [www.pcegenes.ch](http://www.pcegenes.ch) for information.

## tinyBIOS

The tinyBIOS manual can be found at [www.pcegenes.ch/tinybios.htm](http://www.pcegenes.ch/tinybios.htm) . Please note that the BIOS core available on the web site is a bit behind the one used on the WRAP board.

## Literature

Please visit [www.pcegenes.ch/resource.htm](http://www.pcegenes.ch/resource.htm) for pointers to literature and standards. The following are documents I used, you can find similar information in many other documents.